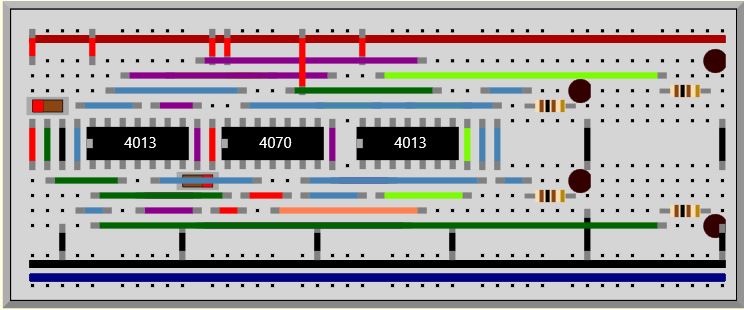
**Design and verify the 4- Bit Synchronous/ Asynchronous Counter using JK flip flop**

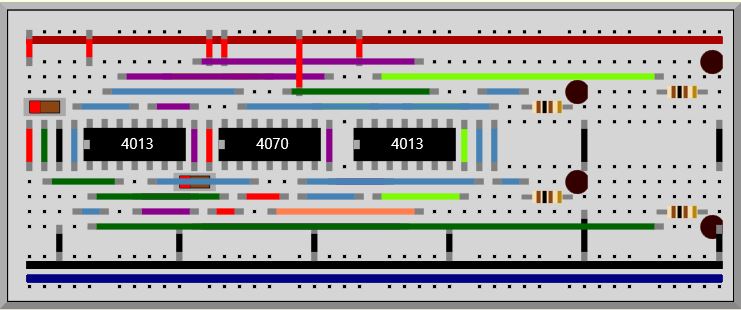
On every pos CLK edge, Output changes.

Asynchronous counter

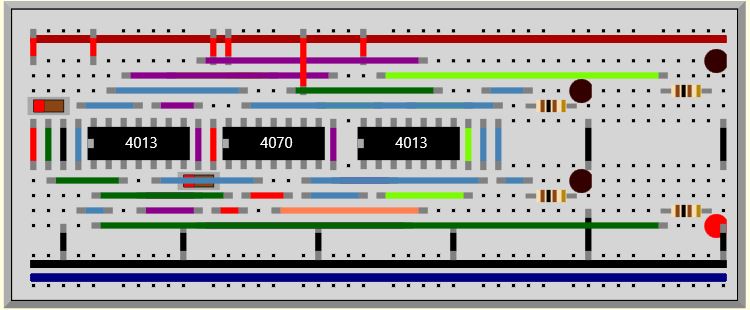
RESET 1



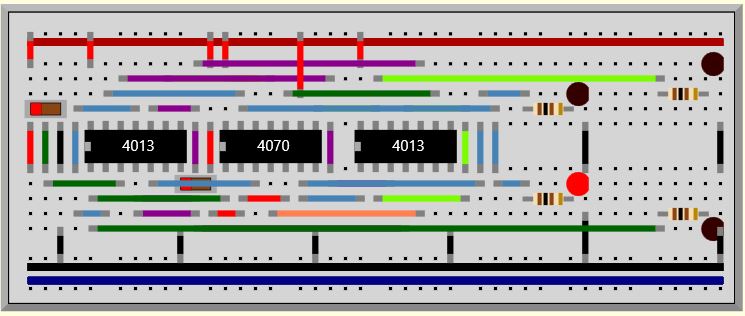
0000



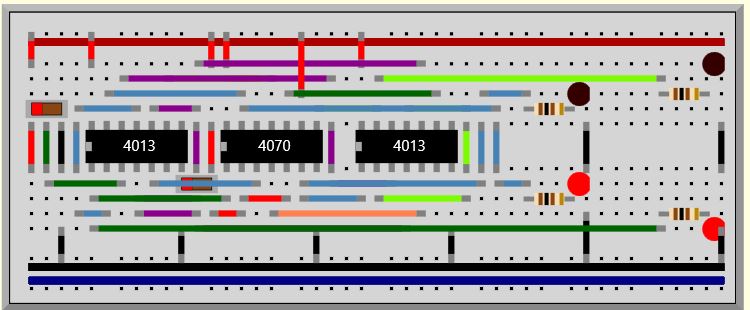
0001



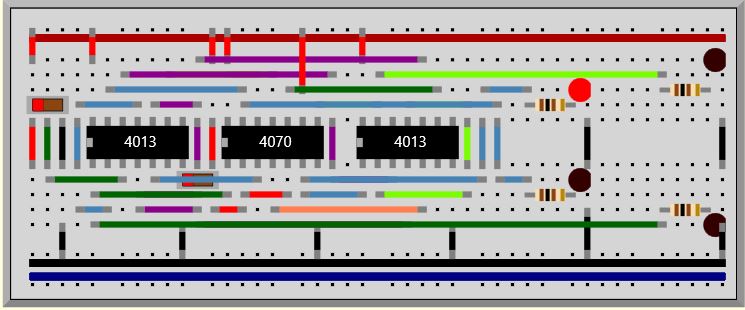
0010



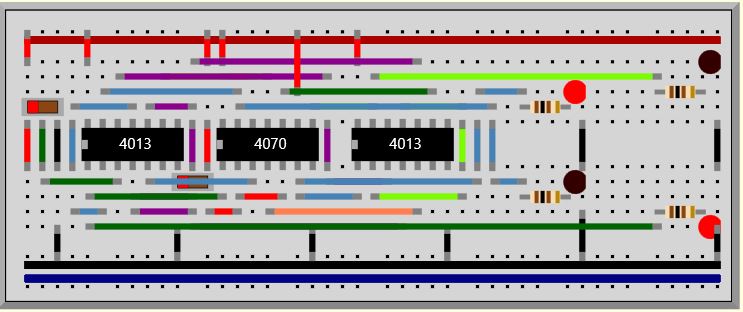
0011



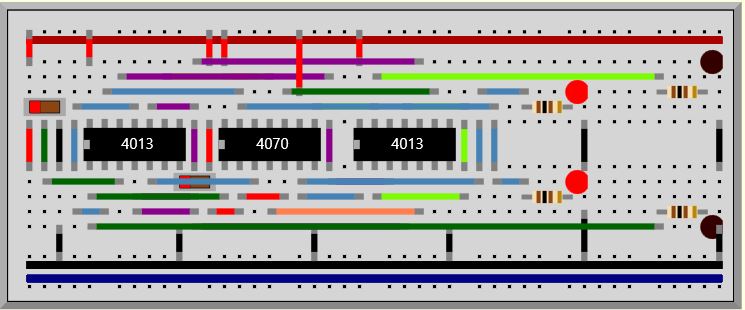
0100



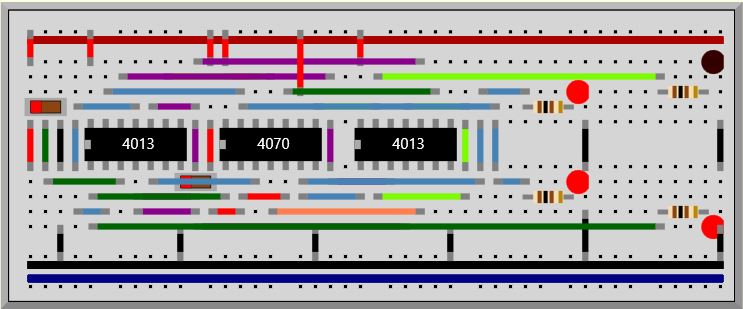
0101



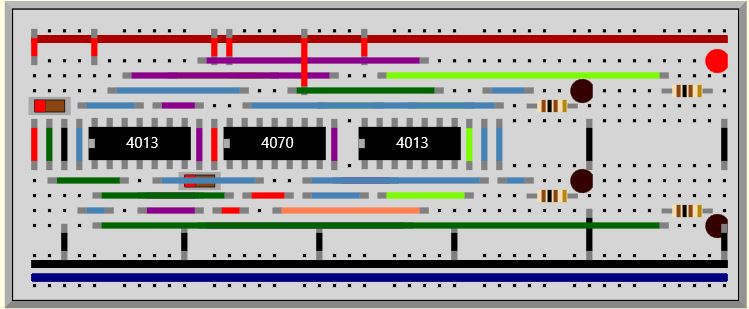
0110



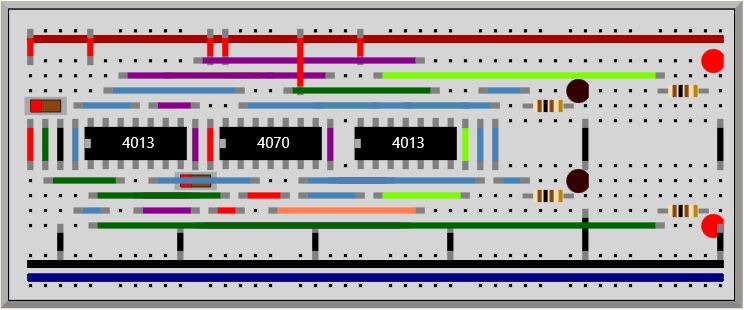
0111



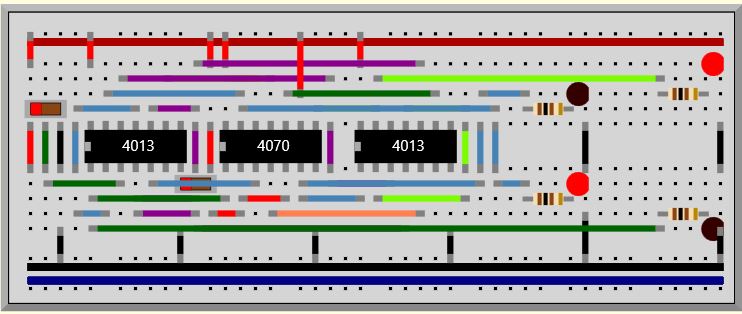
1000



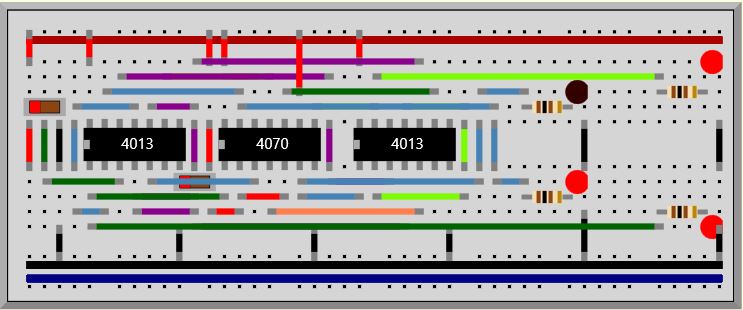
1001



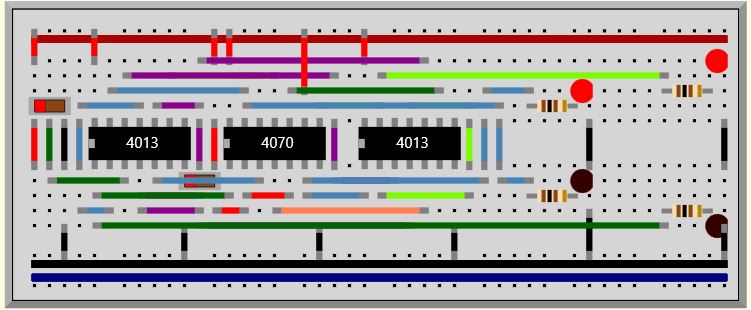
1010



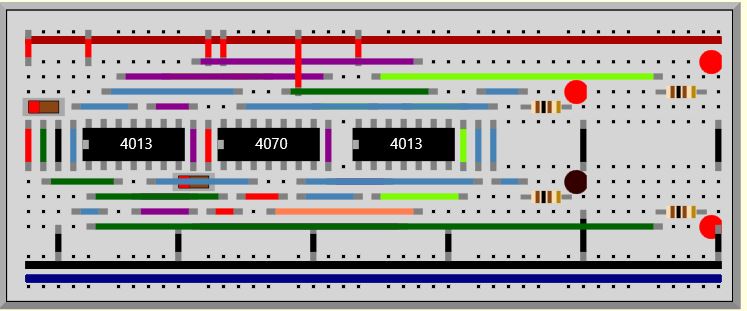
1011



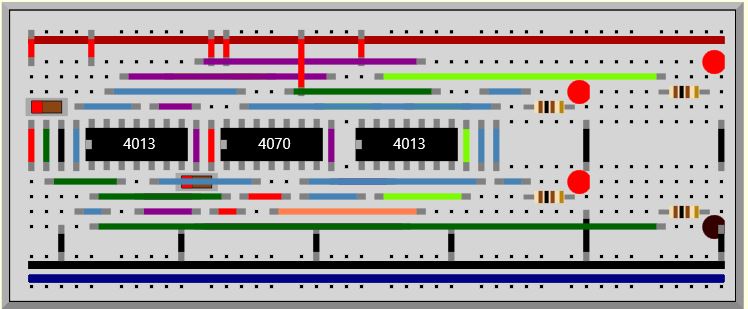
1100



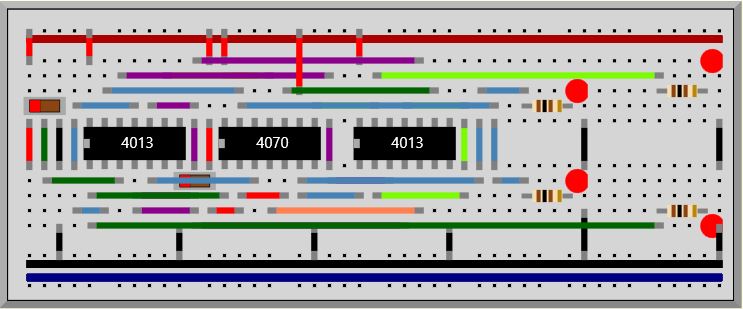
1101



1110

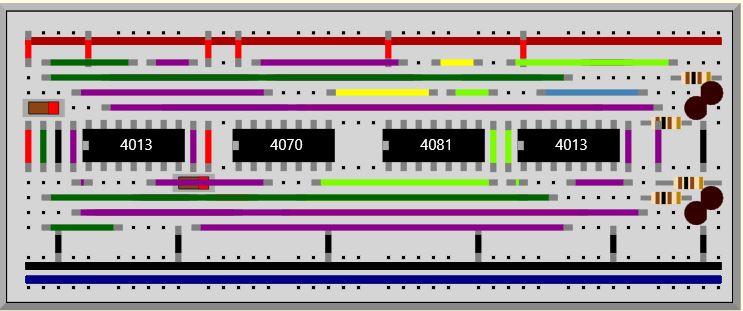


1111

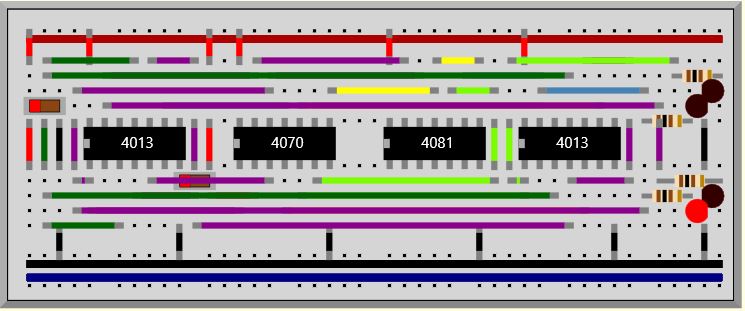


Synchronous

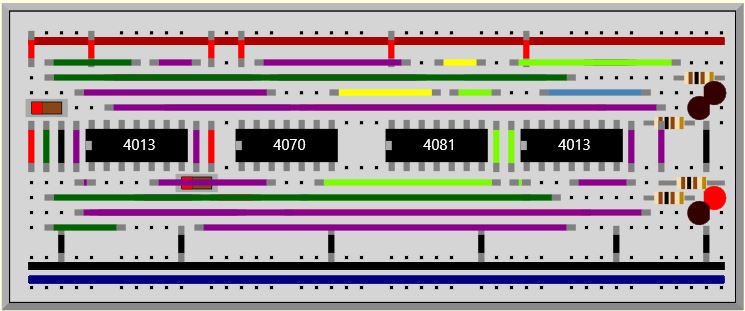
RESET1



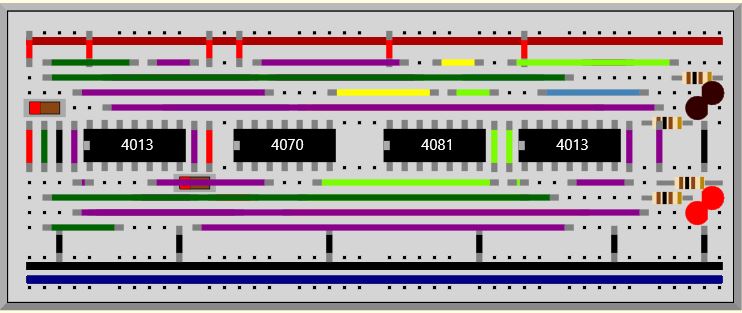
0001



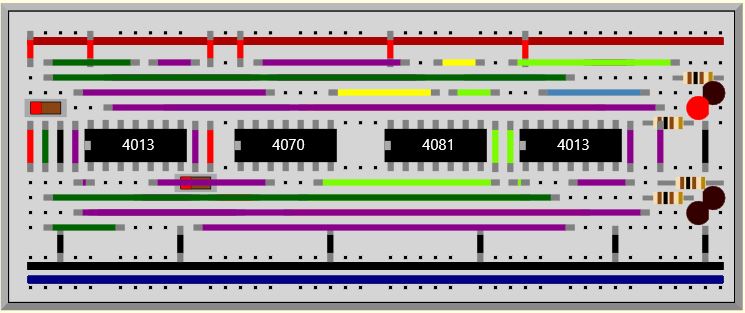
0010



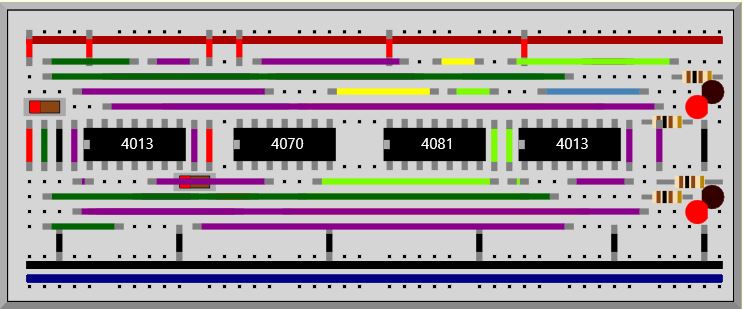
0011



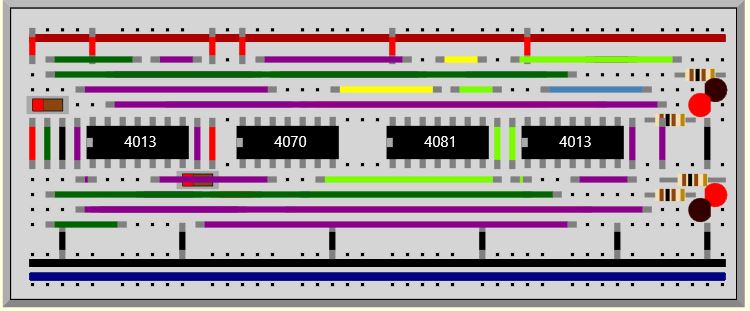
0100



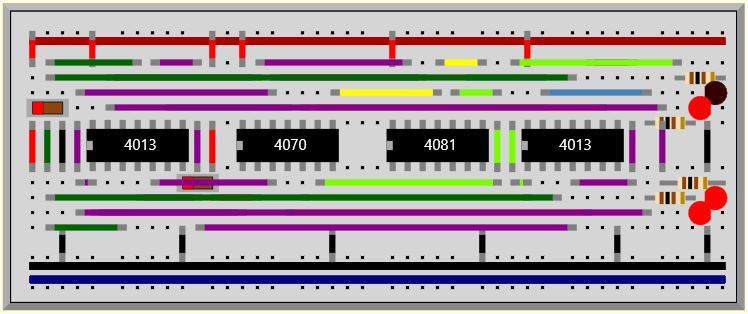
0101



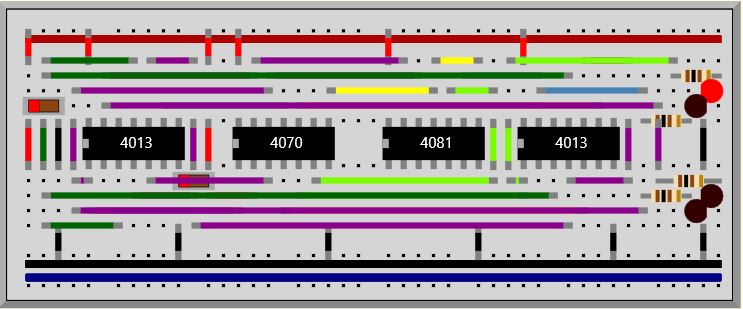
0110



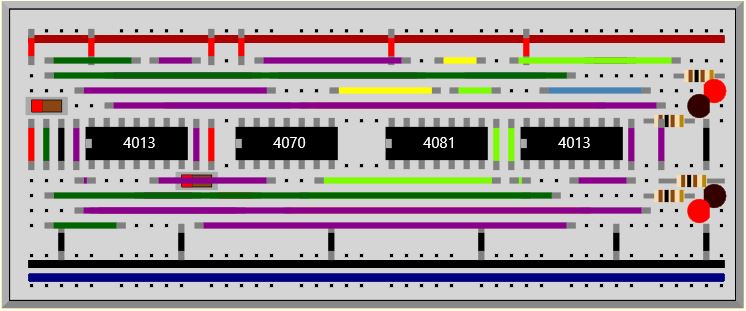
0111



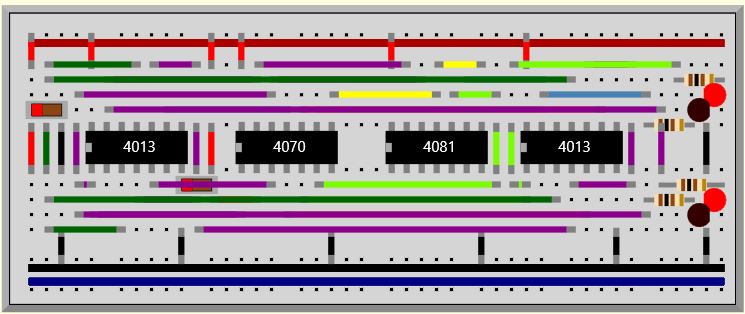
1000



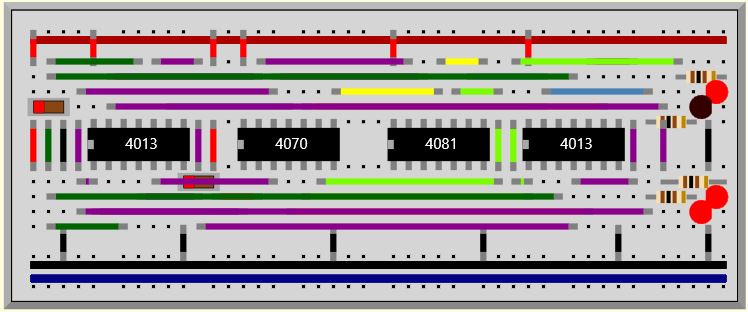
1001



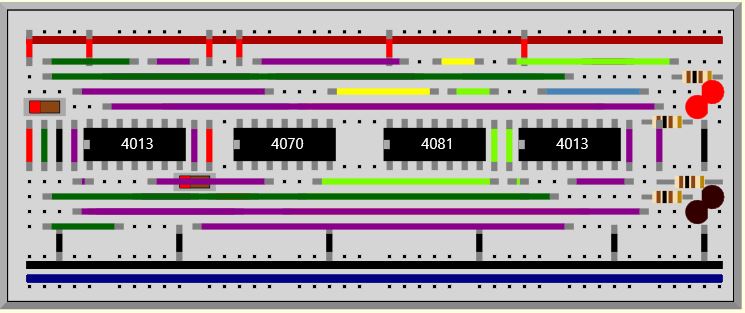
1010



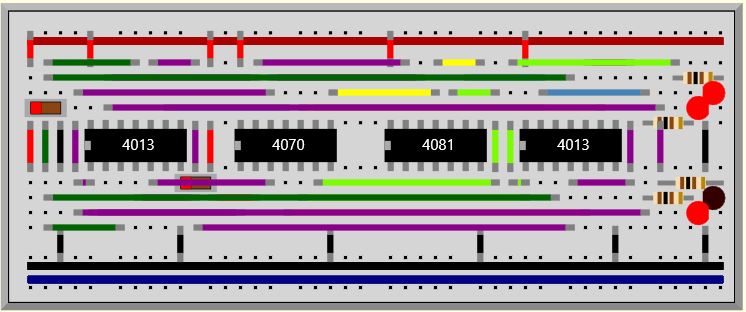
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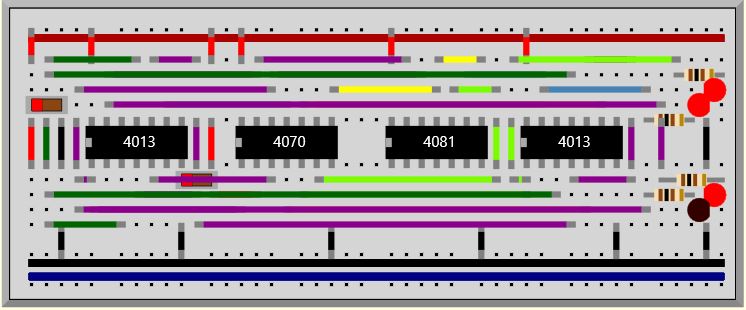
1100



1101



1110



1111

